REMARKS/ARGUMENTS

Claims 13-24 and 26-43 remain pending in this application. Claim 18 is amended as detailed above to clarify the purpose of the variables x and y. In the applicant's respectful submission, the foregoing amendments to claim 18 address the Examiner's objections and introduce no new matter. Claims 13-17, 19-24, and 26-43 have not been amended in this response.

In the applicant's respectful submission, the foregoing amendment does not give rise to any excess claim fees. If necessary, the Commissioner is hereby authorized to charge any fees, including excess claim fees, and any overpayments to Deposit Account No. 13-2400 in this, concurrent, and future replies.

Non Art-Based Rejections

In his Report, the Examiner objected to claims 31, 35 and 41 under 35 U.S.C. 112, first paragraph, on the basis that the subject matter of these claims was not described in the specification at the time the application was filed. In particular, the Examiner states that no support may be found in the application for the use of at least two of the secondary search units to process two distinct addresses in parallel. The applicant has carefully considered the Examiner's rejection, but respectfully traverses the rejection for the reasons that follow.

In the applicant's respectful submission, one of ordinary skill in the art would have appreciated, at the time the application was filed, that the present invention contemplates using the secondary search units to concurrently process distinct addresses. One of the advantages of the present invention is that the first stage is relatively quick and results either in an index or in a pointer to one of the secondary search units. The secondary search units complete the processing of addresses having a prefix longer than the prefix length resolved by the first stage. The interleaved binary tree searching of the secondary search units is a longer process. To avoid a bottle neck, multiple secondary search units are provided in parallel. The application also describes the buffering of addresses that

have been processed through the first stage and are awaiting processing at one of the secondary search units. To avoid a bottle neck at the secondary search units, the present invention teaches that multiple addresses may be processed in parallel at the second stage by different secondary search units.

Support for this aspect of the invention may be found in the detailed description at, for example, page 10, line 25 wherein it states that, "the invention includes one or more of the following concepts; partial address scrambling, concurrent look-up without directory duplication, and encoding interleaved independent (branches) in a shared memory." Additional support may be found at the following locations in the detailed description:

"The search process requires several memory-access steps which increase the translation time". This necessitates the use of **parallel search** as described below.": page 11, lines 22-24.

"It is possible to perform partial indexing followed by **parallel branch searching**. Tree searching requires several memory-access operations per address, but **with several such searches being performed in parallel**, the translation rate (the number of address translations per time unit) can be increased to exceed the rate determined by the single memory-access operation of a one-dimensional indexing stage.": page 11, line 28 to page 12, line 3.

"The searching stage is performed for the remaining bits in an address only when the first stage fails to produce a match. In a preferred form, **the searching stage uses a parallel searching process to increase the speed** as will be described further below.": page 14, lines 5-8.

"Using 16 search units in parallel, and considering that a proportion of address-translation processes may not proceed to the search step, the realizable translation rate would be determined primarily by the first-stage direct indexing step which becomes the bottle neck.": page 17, lines 10-13.

"Scrambling is an attempt to **balance** the storage requirement and the translation **computational effort among a number of parallel translation devices.**", page 18, lines 21-22.

"A number of **searching units may operate in parallel**, so that their **combined speed** equals or exceeds the speed of a single indexing process implementing the column identification.": page 20, lines 1-4.

"Searching is time consuming and the invention provides a solution to circumvent this problem using **parallel searching of non-intersecting segments** of the prefix directory.": page 22, lines 15-17.

With respect to the last quote from the description set out above, the applicant notes that non-intersecting segments of the prefix directory naturally belong to distinct addresses. In view of the foregoing references in the description to the concept of operating the secondary search units in parallel, it would be apparent to one of ordinary skill in the art that the invention contemplates performing concurrent searches in different secondary search units for distinct addresses. Accordingly, the applicant respectfully requests that the Examiner withdraw this rejection.

Art-Based Rejections

In his Report, the Examiner rejected claims 13, 14, 23, 24, 28, 31, 32, 34, 35, and 37-41 as being anticipated by the Lampson reference. For the reasons outlined below, the applicant respectfully traverses the Examiner's rejection and requests that it be withdrawn.

The Lampson reference describes a method of resolving an Internet address. An Internet address generally has a prefix, which defines the network address. The remaining bits form a user's address within a sub-network. The number of bits in a prefix may vary

between 8 and 31.

As noted by Lampson, a convenient method to search for an address within an ordered list of addresses is to use a binary search. The difficulty with using a binary search is that a formal binary search requires that all items in the list be of equal length. A conventional approach to addressing this problem with variable length prefixes is to pad a prefix with zeros in order to make the prefix conform to the prescribed length. Lampson notes the problem that arises when prefixes are simply padded with zeros. Accordingly, he proposes a modified binary search wherein each prefix is padded once with zeros and once with ones to produce a pair of padded prefixes. Each pair of padded prefixes defines a range. Lampson suggests using pointers to keep track of the two prefixes involved in defining the range.

In Section IV, Lampson describes a two stage approach to resolving Internet addresses. Lampson proposes a pre-computed 16-bit prefix table having a best matching prefix and a pointer to a secondary stage table. Lampson proposes performing his modified binary search using a modified binary-search table in which prefixes are encoded as ranges.

As noted at page 1253, under the heading "Search", Lampson suggests a first step of indexing the first 16-bits of the address. If a match is not found, the next 16-bits of the address are used to perform a secondary search using Lampson's modified binary search process.

The search process described by Lampson for resolving Internet addresses is described in the context of its implementation on a general purpose computer. Lampson's search involves a single access to the first indexing table (65,536 entries) followed by his new binary search approach for remaining prefixes. Remaining prefix search is performed in binary search tables stored in a single memory (which is actually the same memory that contains the first memory of 65,536 entries). Having described the implementation of a search process on a general purpose computer, Lampson contemplates a single processor

and a single memory for storing the tables necessary to resolve addresses. As a result of this, Lampson then explores the idea of exploiting the wide cache line to improve the process. The use of a wide cache line is useful to many computational processes that require frequent fetching of data from memory, especially in a general purpose computer. This technique is not specific to address resolution. The cache line fill process that Lampson proposes to use is described in Section V of his paper. He titles this section "Multi-Way" binary search, although his use of this term is not fully explained. What Lampson describes is loading the cache line with multiple keys and pointers so as to reduce the number of memory accesses necessary to perform his modified binary search process.

Lampson does not describe processing more than one address at the same time. Lampson does not describe performing more than one search in parallel. Lampson does not describe more than one secondary search unit. Lampson describes a single search unit performing a single search in a single memory storing an indexing table and one or more binary search tables.

Claim 13

Claim 13 of the present invention is directed to a method of resolving addresses. The method includes a step of accessing table V of the secondary search unit indicated by the pointer using each successive remaining bit of the address in order and accessing table T of the secondary search unit at each successive location corresponding to the location of table V accessed. Lampson neither teaches nor suggests tables V and T, as claimed in the present application, wherein the tables are stored in a secondary search unit and are in one-to-one correspondence to one another. Moreover, Lampson fails to teach or suggest a bit-wise address resolution using tables V and T in the secondary search unit. Accordingly, the applicant respectfully submits that Lampson fails to teach or suggest the elements claimed in claim 13 of the present application, and the applicant respectfully requests that the Examiner withdraw this rejection.

Claim 23

Claim 23 of the present application is directed to an apparatus for address translation of a packet. The apparatus comprises a plurality of secondary search units, each having a memory, for searching in parallel for different prefixes of length greater than A. Claim 23 further specifies that each secondary memory comprises tables V and T containing interleaved tree branches. Lampson fails to teach or suggest a plurality of secondary search units, as described above. Lampson teaches only a single secondary search unit having a single memory. In fact, Lampson teaches a single unit having a single memory for implementing both first and second stages. Lampson does not teach or suggest searching in parallel for different prefixes. Moreover, Lampson fails to teach or suggest tables V and T containing interleaved tree branches. One of ordinary skill in the art would not be inclined to modify the Lampson reference to provide for multiple secondary search units for searching in parallel since Lampson provides no motivation or teaching in this regard. Therefore, the applicant respectfully submits that claim 23 is patentably distinguishable over the Lampson reference and respectfully requests that the Examiner withdraw this rejection.

Claim 28

Claim 28 is directed to an address translation apparatus. The apparatus comprises a plurality of secondary search units for performing secondary searches in parallel. Each secondary search unit having the branch search data structure for performing each secondary search and translating the address to a prefix, if the primary translation table indicates the location of a branch search data structure to begin the secondary search.

As noted above in connection with claim 23, Lampson fails to teach or suggest a plurality of secondary search units for performing secondary searches in parallel. Accordingly, Lampson also fails to teach or suggest a primary translation table containing locations of branch search data structures in secondary search units. Therefore, the applicant respectfully submits that claim 28 of the present application is patentably distinguishable

over the Lampson reference and respectfully requests that the Examiner withdraw this rejection.

Claim 32

Claim 32 is directed to a method of translating addresses including steps of indexing a first memory device containing an indexing table and determining from said indexing a translation code, a first pointer, and a second pointer. Lampson fails to teach or suggest a second pointer resulting from the indexing step. Accordingly, the applicant respectfully submits that claim 32 is patentably distinguishable over the Lampson reference.

Claim 32 also specifies a step of accessing a secondary memory device from among a plurality of secondary memory devices, and performing a tree search process on a tree structure having a root defined by the second pointer. As Lampson fails to teach or suggest a second pointer, Lampson also falls to teach or suggest performing a tree search process, wherein the tree structure has a root defined by the second pointer. Accordingly, the applicant respectfully submits that the Lampson reference neither teaches nor suggests the elements claimed in claim 32 of the present application. The applicant therefore respectfully requests that the Examiner withdraw this rejection.

Claim 37

Claim 37 is directed to a method of resolving addresses that includes a step of resolving a data record to two identifiers if a translation equals a second predetermined value, wherein a first identifier indicates a target secondary search unit and a second identifier indicates a location in a target secondary search unit. Lampson neither teaches nor suggests resolving a data record to two identifiers. Lampson also falls to teach or suggest a plurality of secondary search units. Accordingly, Lampson would not be inclined to provide for an identifier indicating a target secondary search unit. Therefore, Lampson fails to teach or

suggest the elements claimed in claim 37 of the present application. In the applicant's respectful submission, claim 37 is patentably distinguishable over the Lampson reference, and the applicant respectfully requests that the Examiner withdraw this rejection.

Claims 14, 24, 31, 34, 35, and 38-41

The applicant repeats and relies upon the above submissions regarding independent claims 13, 23, 28, 32, and 37 with respect to the rejections made by the Examiner to dependent claims 14, 24, 31, 34, 35, and 38-41. Because the foregoing independent claims are believed to be patentably distinguishable over the Lampson reference, the applicant respectfully submits that all of the dependent claims are also patentably distinguishable over the Lampson reference for substantially the same reasons.

In view of the foregoing amendments and submissions, the applicant respectfully requests the Examiner withdraw his rejections, and the applicant respectfully solicits a timely Notice of Allowance. Should the Examiner have any questions with respect to these submissions, please contact Fraser Rowand at (416) 858-1482.

Respectfully Submitted,
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